



# PIC16C65

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## PIC16C65 Rev. A Silicon Errata Sheet

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The PIC16C65 (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS30234D), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16C65 silicon.

### 1. Module: USART

When the USART (SCI) is configured in asynchronous mode with the BRGH bit set, a high number of receive errors may be experienced. For asynchronous receive operations it is recommended that the USART be configured with the BRGH bit cleared.

**Note:** As with any windowed EPROM device, please cover the window at all times, except when erasing.

# PIC16C65

## Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30234D), the following clarifications and corrections should be noted.

### 1. Module: I/O Ports

The specification for the High Voltage Open Drain I/O (The RA4 pin on most devices) cannot be met without possible long term reliability issues on that I/O pin. If a high voltage drive is required, use an external transistor that can support the required voltage.

**TABLE 1: DC SPECIFICATION CHANGES FROM DATA SHEET**

Param No.	Sym.	Characteristic	New Specification			Data Sheet Specification			Units
			Min	Typ	Max	Min	Typ	Max	
D150	VOD	Open-drain High Voltage	—	—	<b>10</b>	—	—	14	V

### 2. Module: SSP (SPI Mode Timing Specifications)

- a) The SPI interface timings have been modified to the values shown in Table 2.

**TABLE 2: DC SPECIFICATION CHANGES FROM DATA SHEET**

Parm No.	Sym.	Characteristic	New Specification			Data Sheet Specification			Units	
			Min	Typ	Max	Min	Typ	Max		
71	TsCH	SCK input high time (slave mode)	Continuous	1.25T <sub>CY</sub> + 30 ns	—	—	T <sub>CY</sub> + 20 ns	—	—	ns
71A			Single Byte <sup>(1)</sup>	40	—	—	N.A.			ns
72	TsCL	SCK input low time (slave mode)	Continuous	1.25T <sub>CY</sub> + 30 ns	—	—	T <sub>CY</sub> + 20 ns	—	—	ns
72A			Single Byte <sup>(1)</sup>	40	—	—	N.A.			ns
73A	T <sub>B2B</sub>	Last clock edge of the Byte1 to 1st clock edge of the Byte2 <sup>(1)</sup>	1.5 T <sub>CY</sub> + 40 ns	—	—	N.A.			ns	

\* This parameter is characterized but not tested

**Note 1:** Specification 73A is only required if specifications 71A and 72A are used.

### 3. Module: Timer1

- a) The operation of Timer1 needs some clarification when the timer registers are written when the TMR1ON bit is set.

The internal clock signal that is the input to the TMR1 prescaler affects the incrementing of Timer1 (TMR1H:TMR1L registers and the Timer1 prescaler). When the Timer1 registers are NOT written, the Timer1 will increment on the rising edge of the TMR1 increment clock.

When the TMR1H and/or TMR1L registers are written while this clock is high, TMR1 will increment on the next rising edge of this clock.

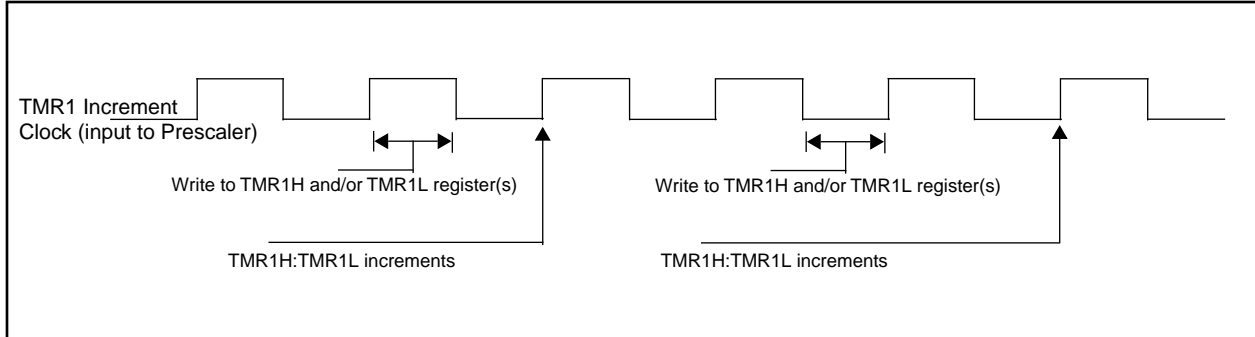
When the TMR1H and/or TMR1L registers are written while this clock is low, TMR1 will not increment on the next rising edge of this clock, but must first have a falling clock and then the rising clock for TMR1 to increment.

Figure 1 shows the two cases of writes to the TMR1H and/or TMR1L registers. Due to the V<sub>IH</sub> and V<sub>IL</sub> thresholds on the oscillator/clock pins, external

Timer1 oscillator components, and external clock frequency, the Timer1 increment clock may not be of a 50% duty cycle.

The TMR1 increment clock is out of phase of the T1OSO/T1CKI pin by a small propagation delay.

**FIGURE 1: WRITES TO TIMER1 (EXTERNAL CLOCK / OSCILLATOR MODE)**



4. Module: RC Oscillator

The table for RC Oscillator Frequencies in the Device Characterization section of the Data Sheet is incorrect. The correct characterization information is shown in Table 3.

**TABLE 3: RC OSCILLATOR FREQUENCIES CHARACTERIZATION CHANGES FROM DATA SHEET**

Cext	Rext	Correct Characterization Data		Current Data Sheet Values	
		Average	% Variation	Average	% Variation
22 pF	5.1 K	3.55 MHz	± 9.63%	4.12 MHz	± 1.4%
	10 K	1.99 MHz	± 10.53%	2.35 MHz	± 1.4%
	100 K	221.9 KHz	± 12.10%	268 KHz	± 1.1%
100 pF	3.3 K	1.77 MHz	± 10.67%	1.80 MHz	± 1.0%
	5.1 K	1.22 MHz	± 10.41%	1.27 MHz	± 1.0%
	10 K	669.4 KHz	± 10.92%	688 KHz	± 1.2%
	100 K	71.5 KHz	± 11.21%	77.2 KHz	± 1.0%
330 pF	3.3 K	625.1 KHz	± 10.68%	707 KHz	± 1.4%
	5.1 K	428.5 KHz	± 10.96%	501 KHz	± 1.2%
	10 K	231.9 KHz	± 11.32%	269 KHz	± 1.6%
	100 K	24.4 KHz	± 12.93%	28.3 KHz	± 1.1%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from the average value for Vdd = 5V



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5925 Airport Road, Suite 200  
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### ASIA/PACIFIC

#### Hong Kong

Microchip Asia Pacific  
Unit 2101, Tower 2  
Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T., Hong Kong  
Tel: 852-2-401-1200 Fax: 852-2-401-3431

#### Beijing

Microchip Technology, Beijing  
Unit 915, 6 Chaoyangmen Bei Dajie  
Dong Erhuan Road, Dongcheng District  
New China Hong Kong Manhattan Building  
Beijing 100027 PRC  
Tel: 86-10-85282100 Fax: 86-10-85282104

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India Liaison Office  
No. 6, Legacy, Convent Road  
Bangalore 560 025, India  
Tel: 91-80-229-0061 Fax: 91-80-229-0062

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Microchip Technology Intl. Inc.  
Benex S-1 6F  
3-18-20, Shinyokohama  
Kohoku-Ku, Yokohama-shi  
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Tel: 81-45-471-6166 Fax: 81-45-471-6122

#### Korea

Microchip Technology Korea  
168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku  
Seoul, Korea  
Tel: 82-2-554-7200 Fax: 82-2-558-5934

#### Shanghai

Microchip Technology  
RM 406 Shanghai Golden Bridge Bldg.  
2077 Yan'an Road West, Hong Qiao District  
Shanghai, PRC 200335  
Tel: 86-21-6275-5700 Fax: 86 21-6275-5060

### ASIA/PACIFIC (continued)

#### Singapore

Microchip Technology Singapore Pte Ltd.  
200 Middle Road  
#07-02 Prime Centre  
Singapore 188980  
Tel: 65-334-8870 Fax: 65-334-8850

#### Taiwan, R.O.C

Microchip Technology Taiwan  
10F-1C 207  
Tung Hua North Road  
Taipei, Taiwan, ROC  
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

### EUROPE

#### United Kingdom

Arizona Microchip Technology Ltd.  
505 Eskdale Road  
Wokingham  
Berkshire, England RG41 5TU  
Tel: 44 118 921 5858 Fax: 44-118 921-5835

#### Denmark

Microchip Technology Denmark ApS  
Regus Business Centre  
Lautrup hof 1-3  
Ballerup DK-2750 Denmark  
Tel: 45 4420 9895 Fax: 45 4420 9910

#### France

Arizona Microchip Technology SARL  
Parc d'Activite du Moulin de Massy  
43 Rue du Saule Trapu  
Batiment A - 1er Etage  
91300 Massy, France  
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

#### Germany

Arizona Microchip Technology GmbH  
Gustav-Heinemann-Ring 125  
D-81739 München, Germany  
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

#### Italy

Arizona Microchip Technology SRL  
Centro Direzionale Colleoni  
Palazzo Taurus 1 V. Le Colleoni 1  
20041 Agrate Brianza  
Milan, Italy  
Tel: 39-039-65791-1 Fax: 39-039-6899883

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